What is claimed is:

1. An apparatus for restoring cell sequence in a switch fabric, which comprises:

a first registering means for temporarily storing an input cell;

a second registering means for storing virtual channel identifier (VCI) values for a plurality of cells including the input cell provided from the first registering means and outputting each of the VCI values after a predetermined cell time; and

logical queuing means for sorting the cells based on their VCI and time stamp values to thereby place each of the cells at a proper position in a corresponding logical queue, and outputting said each of the cells in response to the outputted VCI value, wherein cells having a same VCI value are arranged in one corresponding logical queue according to the order of their time stamp values.

2. The apparatus as recited in claim 1, wherein the logical queuing means includes:

a buffering means for storing the cells in corresponding logical queues until the cells are outputted;

a storage means for containing a VCI value corresponding to said each of the logical queues and a buffer address representing a position of a head cell in

said each of the logical queues; and

a controlling means for managing an input and output process of the buffering means based on the VCI and time stamp values of the cells.

3. The apparatus as recited in claim 2, wherein the logical queuing means further includes an idle address providing means for supplying an idle address of the buffering means to the controlling means upon arrival of the input cell, wherein an address of an outputted cell is transmitted to the idle address providing means and treated as the idle address.

4. The apparatus as recited in claim 2, wherein the storage means contains:

a content addressable memory (CAM) for storing the VCI value corresponding to said each of the logical queues; and

a random access memory (RAM) for storing the buffer address representing the position of the head cell in said each of the logical queues.

5. The apparatus as recited in claim 4, wherein the buffering means contains:

a cell data field (CDF) for storing the cells and the time stamp values of the cells; and

a next address field (NAF) for storing addresses of

successive cells in said each of the logical queues.

6. The apparatus as recited in claim 5, wherein, if the input cell is provided, the controlling means performs the input process of the buffering means through the steps of:

(a1) examining whether the same VCI value as that of the input cell exists in the CAM part of the memory table;

(a2) if the storage means contains no VCI value corresponding to the input cell, registering a new VCI value in the CAM part and writing a new buffer address of the input cell on the RAM part of the storage means, wherein the input cell is treated as a head cell of a new logical queue corresponding to the new VCI value; and

(a3) if the CAM part of the storage means contains the same VCI value as that of the input cell, receiving the buffer address of the head cell of the logical queue corresponding to the VCI value of the input cell, reading a time stamp value of the head cell from the CDF by using the buffer address of the head cell and the address of the subsequent cell from the NAF, and finding the proper position of the input cell to thereby place the input cell at the proper position by comparing the time stamp value of the input cell with those of the cells stored in the buffering means.

7. The apparatus as recited in claim 6, wherein, if the

storage means contains no VCI value corresponding to the input cell, the input cell and its time stamp value are transferred from the first registering means to the CDF of the addressed position in response to said new buffer address and an end of logical queue (EOL) mark is written on the NAF.

8. The apparatus as recited in claim 7, wherein the controlling means performs the output process of the buffering means through the steps of:

(b1) receiving a VCI value shifted out from the second registering means;

(b2) receiving an address of a head cell of a logical queue corresponding to said VCI value from the storage means; and

(b3) outputting said head cell pointed by the address and designating a subsequent cell of said head cell as a new head cell in the logical queue.

9. The apparatus as recited in claim 4, wherein the buffering means contains:

a first field for storing the cells and extracting the cells by the controlling means; and

a second field for storing the time stamp values and addresses of successive cells in said each of the logical queues.

10. The apparatus as recited in claim 9, wherein, if the input cell is provided, the controlling means performs the input process of the buffering means through the steps of:

(c1) examining whether the same VCI value as that of the input cell exists in the CAM part of the memory table;

(c2) if the storage means contains no VCI value corresponding to the input cell, registering a new VCI value in the CAM part and writing a new buffer address of the input cell supplied from the idle address providing means on the RAM part of the storage means, wherein the input cell is treated as a head cell of a new logical queue corresponding to the new VCI value; and

(c3) if the CAM part of the storage means contains the same VCI value as that of the input cell, receiving the buffer address of the head cell of the logical queue corresponding to the VCI value of the input cell, reading a time stamp value of the head cell and the address of the subsequent cell from the second field by using the buffer address of the head cell, and finding the proper position of the input cell to thereby place the input cell at the proper position by comparing the time stamp value of the input cell with those of the cells stored in the buffering means.

11. The apparatus as recited in claim 10, wherein, if the storage means contains no VCI value corresponding to the

input cell, the input cell and its time stamp value are transferred from the first registering means to the addressed position in the buffering means in response to said new buffer address and an end of logical queue (EOL) mark is written on the second field.

12. The apparatus as recited in claim 11, wherein the controlling means performs the output process of the buffering means through the steps of:

(d1) receiving a VCI value shifted out from the second registering means;

(d2) receiving an address of a head cell of a logical queue corresponding to said VCI value from the storage means; and

(d3) outputting said head cell pointed by the address.

13. The apparatus as recited in claim 1, wherein the predetermined cell time is V cell times, V being a difference between the minimum and the maximum permissible transfer delay within the switch fabric.

14. A method for restoring cell sequence in a switch fabric, which comprises the steps of:

(a) examining a virtual channel identifier (VCI) value of an input cell and transmitting the input cell to a logical queue that has a same VCI as that of the input cell;

(b) placing the input cell at a proper position in the logical queue by comparing a time stamp value of the input cell with those of cells stored in the logical queue;

(c) repeating the steps (a) and (b) for a plurality of input cells;

(d) selecting a head cell among the cells stored in the logical queue by using the VCI value of the input cell as an index after a predetermined cell time;

(e) outputting the head cell as an output cell; and

(f) repeating the steps (d) and (e) for the remaining cells among the input cells.

15. The method of claim 14, wherein the predetermined cell time is V cell times, V being a difference between the minimum and the maximum permissible transfer delay within the switch fabric.